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Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356)**

Question No: 2 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► **Current state and external input (Page 318)**
- ► Input and clock signal applied

Question No: 3 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 299)**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 4 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221)**
- ► False

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Question No: 5 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 6 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 7 (Marks: 1) - Please choose one
_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 8 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369)**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 9 (Marks: 1) - Please choose one
A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter
- ► **Mod-10 counter (Page 274)**

Question No: 10 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356)**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

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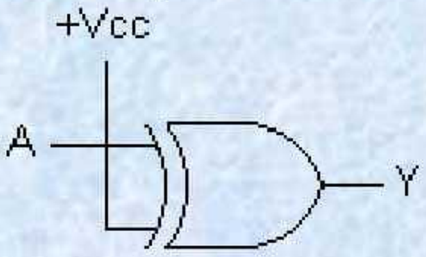
Question No: 11 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- 2
- **4 (Page 394)**
- 8
- 16

Question No: 12 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- 1
- 0
- **A** **Click here for detail**
- $\overline{A}$

Question No: 13 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- 1110
- 1100
- 1000
- **0000 (Page 34)**

Question No: 14 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- **Vout / Vin = - Rf / Ri (Page 446)**
- Vout / Rf = - Vin / Ri
- Rf / Vin = - Ri / Vout
- Rf / Vin = Ri / Vout

Question No: 15 (Marks: 1) - Please choose one
LUT is acronym for _____

- **Look Up Table (Page 439)**
- Local User Terminal
- Least Upper Time Period
- None of given options

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Question No: 16 (Marks: 1) - Please choose one
The three fundamental gates are _____
- ► AND, NAND, XOR
- ► OR, AND, NAND
- ► NOT, NOR, XOR
- ► **NOT, OR, AND (Page 40)**

Question No: 17 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____
- ► The organization of memory
- ► The structure of memory
- ► The size of decoding unit
- ► **The size of the address bus of the microprocessor (Page 430)**

Question No: 18 (Marks: 1) - Please choose one
Stack is an acronym for _____
- ► FIFO memory
- ► **LIFO memory (Page 429)**
- ► Flash Memory
- ► Bust Flash Memory

Question No: 19 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____
- ► 213
- ► 123
- ► **127**
- ► 345

Question No: 20 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.
- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 21 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
- ► Race condition
- ► **Clock Skew (Page 226)**
- ► Ripple Effect
- ► None of given options

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Question No: 22 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

- ► 0000
- ► **1101 (not sure)**
- ► 1011
- ► 1111

Question No: 23 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- ► **Current state and the inputs (Page 332)**
- ► Current state and outputs
- ► Previous state and inputs
- ► Previous state and outputs

Question No: 24 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335)**

Question No: 25 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► 1100
- ► 0011
- ► **0000 Click here for detail**
- ► 1111

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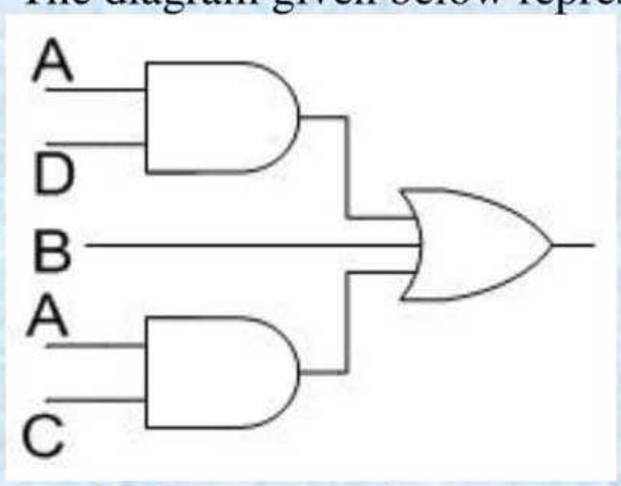
Question No: 27 (Marks: 1) - Please choose one
LUT is acronym for _____

- **Look Up Table (Page 439) rep**
- Local User Terminal
- Least Upper Time Period
- None of given options

. Question No: 28 (Marks: 1) - Please choose one
The diagram given below represents _____



- Demorgans law
- Associative law
- Product of sum form
- **Sum of product form (Page 78)**

Question No: 29 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- **Doesn't have an invalid state (Page 232)**
- Sets to clear when both J = 0 and K = 0
- It does not show transition on change in pulse
- It does not accept asynchronous inputs

Question No: 30 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

- Serial data to parallel
- **Parallel data to serial (Page 356) rep**
- Serial data to serial
- Parallel data to parallel

Question No: 31 (Marks: 1) - Please choose one
A GAL is essentially a _____.

- Non-reprogrammable PAL
- PAL that is programmed only by the manufacturer
- Very large PAL
- **Reprogrammable PAL (Page 183)**

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Question No: 32 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► **FAST Mode Page Access (Page 413)**
- ► None of given options

Question No: 33 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 34 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

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